REMARKS

Claims 1 and 3-18 are pending in the application. Claims 1, 7 and 13-15 have been amended and new claims 16-18 have been added by way of the present amendment. Reconsideration is respectfully requested.

In the outstanding Office Action, claims 1, 3-6 and 13-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Applicant's Prior Art (APA) of **FIG. 2B** in view of U.S. Publication No. 2002/0122280 A1 (Ker et al. I) and U.S. Patent No. 6,194,776 (Amano et al.); claims 7, 8, and 10-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the APA of **FIG. 2B** in view of U.S. Patent No. 6,566,715 B1 (Ker et al. II); and claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over APA of **FIG. 2B** in view of Ker et al. II as applied to claim 7 above, and further in view of Ker et al. I. Reconsideration is respectfully requested.

35 U.S.C. § 103 Claim Rejections

Claims 1, 3-6 and 13-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the APA of **FIG. 2B** in view of Ker et al. I and Amano et al. Applicants respectfully traverse the outstanding rejection.

Claims 1, 7 and 13 have been amended to clarify the invention. In particular, claim 1 has been amended to recite:

> a substrate having first, second and third wells formed in said substrate, ~~and~~ separated by shallow ~~well~~ trench isolation ~~regions~~ structures, and generally separating the bottom of said ~~second~~ first well from said substrate with a segmented conductive band;
>
> a source and drain region in said ~~second~~ first well forming an FET, said drain being connected to an I/O pad for protecting said pad against an ESD event; and

a path of substrate material extending through an opening in said segmented conductive band ~~region, increasing the~~ configured to increase substrate resistance in the path ~~of the~~ for current which flows through said I/O pad to a substrate contact and drain during an ESD event and electrically connecting the ~~second~~ first well to the substrate,

wherein the ~~first~~ second and third wells are completely isolated from the drain, source and substrate contact by the shallow trench isolation structures, and

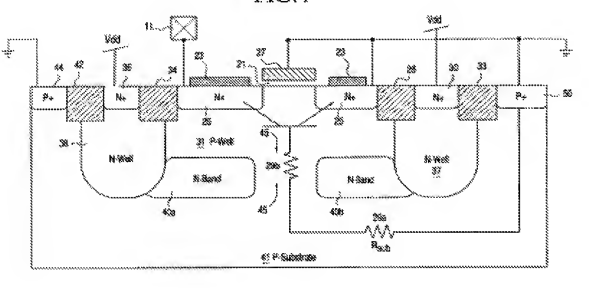
wherein the substrate contact is located outside the first, second and third wells and directly connected to the substrate.

wherein the first and third wells are completely isolated from the drain, source and substrate contact, and

wherein the substrate contact is located outside the first, second and third wells and directly connected to the substrate.

Claims 7 and 13 have been amended in a similar manner. Support for the amendment is provided by the published application; and shown at least in the replacement sheet for amended **FIG. 4**, as shown below. In particular, paragraph **[0027]** recites:

FIG.4



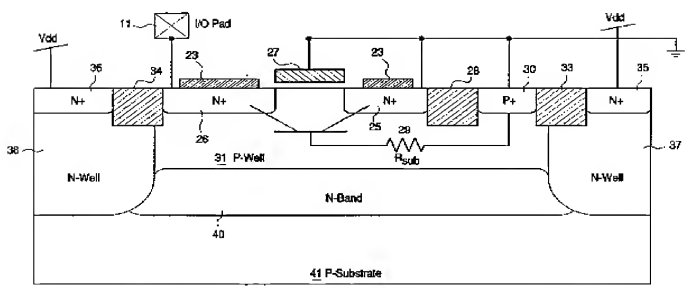
N-well contacts **30**, **36**, source **25**, drain **26** and substrate contacts **44** and **50** are isolated from each other using shallow trench isolation structures **28**, **33**, **34** and **42**. P-well **31** is generally separated from the substrate **41** with a segmented N-band

> conductive band region **40a**, **40b**. N-well **38** and N-well **37** are connected through contact **36, 30** to **VDD**. As shown in the figure, an opening **45** is provided between N-band segments **40a** and **40b** through which P-well **31** is electrically connected to the substrate **41**. The result is a resistive path from P-well **31**, represented as **29a** and **29b**, to a substrate contact **44** and **50** located outside of the N-wells.[1]

In addition, new claims 16-18 have been added by way of the present amendment. Support for the new claims is shown at least in **FIG. 4**, reference **23** and provided at least at paragraph **[0026]** of the published application which recites: "[s]ource and drain silicide blocked regions 23 are formed over the source and drain."[2] Therefore, the amendments raise no questions of new matter.

The APA discloses the implementation of an ESD NMOSFET in a triple well CMOS architecture.[3] In particular, a shown in **FIG. 2B** below, the APA discloses an additional

FIG.2B



[1] U.S. Patent Application Publication No. US 2005/0224882 at least at page 3, paragraph **[0027],** lines 11-12; and **FIG. 4**, at references **28, 33, 34, 42, 44** and **50.**

N-Band **40** that constitutes an n-type doped region which in combination with the N-Wells **37** and **38** isolates the P-well **31** from the substrate **41**.[4] As can be seen from **FIG. 2B** of the, this triple well architecture of the APA is similar to the dual well architecture of the background, *with the exception of the additional N-Band **40**, and N-wells **37** and **38**.*[5] N-wells **37** and **38** are connected in the embodiment shown in **FIG. 2B** to a positive potential Vdd.[6] Additionally, two isolation regions **33** and **34** provide isolation for N-well **37** and N-well **38** from the P+ substrate contact **30** and N+ drain contact **26**, respectively.[7]

However, the APA of **FIG. 2B** above nowhere discloses, as recited in amended claims, 1:

> *a path of substrate material extending through an opening in said segmented conductive band configured to increase substrate resistance in the path for current which flows through said I/O pad to a substrate contact and drain* during an ESD event and electrically connecting the first well to the substrate,
>
> wherein *the second and third wells are completely isolated from the drain, source and substrate contact by the shallow trench isolation structures*, and
>
> *wherein the substrate contact is located outside the first, second and third wells and directly connected to the substrate.*
>
> (emphasis added).

That is, the APA of **FIG. 2B** nowhere discloses: a path of substrate material **29b** extending through an opening **45** in said segmented conductive band **40a, 40b**, configured to increase substrate resistance in the path for current which flows through said I/O pad **11** to a substrate contact **50** and drain **26**, as similarly recited in amended claims 1, **7** and 13 and as shown in the replacement sheet for amended **FIG. 4** above. In addition, the APA of **FIG. 2B** nowhere discloses: the second **37** and third **38** wells are completely isolated from the drain **26**, source **25** and substrate contact **44, 50** by the shallow trench isolation structures **28, 33, 34, 42**, as similarly

---

[2] U.S. Patent Application Publication No. US 2005/0224882 at least at page 3, paragraph **[0026]**; and **FIG. 4**, at reference **23.**
[3] *Id.* at page 2, paragraph [0024], lines 1-2.
[4] *Id.* at page 2, paragraph [0024], lines 2-5.
[5] *Id.* at page 2, paragraph [0024], lines 5-8.
[6] *Id.* at page 2, paragraph [0024], lines 8-10.
[7] *Id.* at page 2, paragraph [0024], lines 10-12.

recited in amended claims 1, 7 and 13 and as shown in the replacement sheet for amended **FIG. 4** above. Moreover, the APA of **FIG. 2B** nowhere discloses: the substrate contact **50** is located outside the first **31**, second **37** and third **38** wells and directly connected to the substrate **41**, as similarly recited in amended claims 1, 7 and 13 and as shown in the replacement sheet for amended **FIG. 4** above. Therefore, it is respectfully submitted that the APA of **FIG. 2B** does not disclose the claimed invention.

In addition, the outstanding Office Action acknowledges deficiencies in the APA of **FIG. 2B** and attempts to overcome these deficiencies by combining the APA of **FIG. 2B** with Ker et al. I and Amano et al. However, Ker et al. I and Amano et al. cannot overcome all of the deficiencies of the APA of **FIG. 2B**, as will be discussed below.

Ker et al. I discloses an electrostatic discharge (ESD) protection component with a deep-N-well structure in CMOS technology, as shown in **FIG. 5** below.[8] In particular, discloses that the PNPN structure of the NSCR is composed of the P+ diffusion **52**, the N-well **42**, the P-well **40** and the N+ diffusion **46**.[9] The P+ diffusion **52** is used as the anode of the NSCR device and an NMOS is inserted into the P-well **40**.[10] The drain of the NMOS is formed by the N+ diffusion **44** at the P-N junction of the P-well **40** and the N-well **42**.[11]

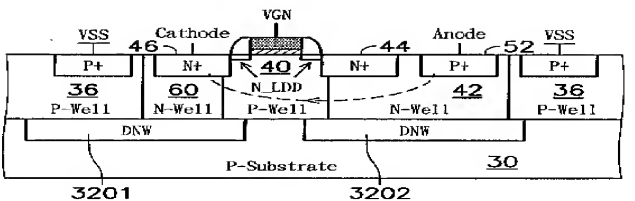
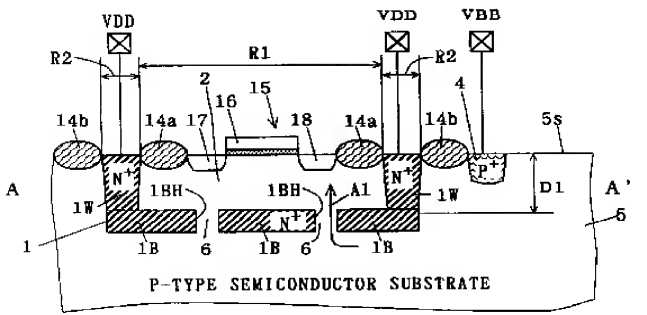


FIG. 5

[8] Ker et al. I at ABSTRACT.
[9] *Id.* at page 3, paragraph [0047], lines 4-6.
[10] *Id.* at page 3, paragraph [0047], lines 6-8.
[11] *Id.* at page 3, paragraph [0047], lines 8-10.

Amano et al. discloses a semiconductor circuit device having a triple-well structure wherein a predetermined potential level is supplied to a top well without a contact region formed in the top.[12] In particular, as shown in **FIG. 1** below, Amano et al. discloses a P-type semiconductor substrate **5**; insulation layer portions **14a, 14b**; a P-type well region **2**; a first source/drain region **17** and a second drain/source region **18**; an N+ well region **1** includes a sidewall portion **1W**, wherein the N+ well region **1** further includes a bottom portion 1B coupled to the ring-shaped sidewall portion **1W** to substantially close the bottom surface of the P-type well region **2** except conduction regions **6** of the same conductivity type as the P-type well region **2** and semiconductor substrate **5** that may establish electrical connection between the P-type well region **2** and the semiconductor substrate **5**; and the potential VBB is supplied from the exterior to the contact region **4** while the electrical connection is established between the P-type well region **2** and the P-type semiconductor substrate **5** through the portions **6** having P-type properties and serving as a conduction path. Further, the P-type portion **6** establishes electrical connection between a P-type well region **2** and the semiconductor substrate **5** to permit the potential applied to a contact region **4** to be supplied to the well region **2**.

F I G. 1



Moreover, Amano et al. discloses the conduction regions **6** provided in the N+ type well region **1** are located immediately under the source/drain regions **17** and **18** and that such an arrangement presents a new problem in that the potential level of the source/drain regions **17** and **18** are varied which might cause the NMOS transistor **15** to malfunction and that the same is true for the conduction region positioned *just under a channel region immediately underlying the gate* layer **16** of the NMOS transistor **15** (emphasis added). To solve this problem, Amano et al. discloses the conduction regions **6** must be provided immediately under other than the transistor regions **16**, **17**, and **18**.

However, neither of Ker et al. I or Amano et al. discloses, as recited in amended claims, 1:

> *a path of substrate material extending through a single opening in said segmented conductive band configured to increase substrate resistance in the path for current which flows through said I/O pad to substrate contacts and the drain during an ESD event* and electrically connecting the first well to the substrate,
>
> wherein the second and third wells are completely isolated from the drain, source *and substrate contacts by the shallow trench isolation structures*, and
>
> *wherein the substrate contacts are located outside the first, second and third wells and directly connected to the substrate.* (emphasis added).

That is, neither Ker et al. I or Amano et al. disclose: a path of substrate material **29b** extending through a single opening **45** in said segmented conductive band **40a, 40b**, configured to increase substrate resistance in the path for current which flows through said I/O pad **11** to substrate contacts **45, 50** and the drain **26**, as similarly recited in amended claims 1, 7 and 13 and as shown in the replacement sheet for amended **FIG. 4** above. In addition, neither Ker et al. I or Amano et al. disclose: the second **37** and third **38** wells are completely isolated from the drain **26**, source **25** and substrate contacts **44, 50** by the shallow trench isolation structures **28, 33, 34, 42**, as similarly recited in amended claims 1, 7 and 13 and as shown in the replacement sheet for

[12] Amano et al. at ABSTRACT.

amended **FIG. 4** above. Further, neither Ker et al. I or Amano et al. disclose: the substrate contacts **44**, **50** is located outside the first **31**, second **37** and third **38** wells and directly connected to the substrate **41**, as similarly recited in amended claims 1, 7 and 13 and as shown in the replacement sheet for amended **FIG. 4** above. Furthermore, neither Ker et al. I or Amano et al. disclose "shallow trench isolation structures." Moreover, neither Ker et al. I or Amano et al. disclose more than *one* substrate contact. The claimed invention discloses a plurality of contacts by reciting: "substrate contacts."

Further, it is respectfully submitted that, as discussed above, Amano et al. teaches away from the configuration of the claimed invention by stating: "the conduction regions **6** *must* be provided immediately under *other than the transistor regions **16, 17, and 18***," where 16, 17 and 18 correspond to source/drain, gate, and drain/source, respectively. Moreover, it is respectfully submitted that neither Ker et al. I or Amano et al. disclose, as recited in new claims 17-19: "silicide blocked regions are formed over source and drain."

Thus, in consideration of the discussion above, it is respectfully submitted that neither Ker et al. I or Amano et al. can overcome all of the deficiencies of the APA of **FIG. 2B**. Therefore, it is respectfully submitted that none of the APA of **FIG. 2B** , Ker et al. I or Amano et al., whether taken alone or in combination, discloses, suggest or makes obvious the claimed invention and that claims 1, 3-6 and 13-18 patentably distinguish thereover.

Claims 7, 8, and 10-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the APA of **FIG. 2B** in view of Ker et al. II. Reconsideration is respectfully requested.

As indicated above, amended claim 7 includes similar language to that found in amended claim 1. Thus, at least for the reasons discussed above for claim 1, the APA of **FIG. 2** also does not disclose all of the limitations of claim 7.

The outstanding Office Action acknowledges deficiencies in the APA of **FIG. 2** and attempts to cure those deficiencies with Ker et al. II. However, Ker et al. II cannot overcome all of the deficiencies of the APA of **FIG. 2,** as discussed below.

Ker et al. II discloses a substrate-triggered technique to effectively improve the ESD robustness of integrated circuit (IC) products.[13] In particular, Ker et al. II discloses a substrate-triggered NMOS is positioned in a p-well **32** on a p-substrate **30**.[14] Two poly-silicon gates **34**, serving as the gate (electrode) of the substrate-triggered NMOS, are positioned above the p-well **32**.[15] Two n+ doped regions **36**, functioning as the drain (electrode) of the substrate-triggered NMOS, are positioned between poly-silicon gates **34** on the surface of the p-well **32**.[16] Between the n+ doped regions **36**, a p+ doped region **40** is positioned for the electrical connection to p-well **32** and serves as the trigger node for the substrate-triggered NMOS.[17] Isolation object(s) **42**, in this example, the silicon oxide formed by the shallow trench isolation processes, isolate the p+ doped region **40** from the n+ doped regions **36**.[18] The two n+ doped regions **38** on the surface(s) of p-well(s) 32 provide the source (electrode) of the substrate-triggered NMOS.[19] As shown in FIG. 5B, one of the n+ doped regions **38**, a p-well **32** and one of the n+ doped region 36 together can construct a parasitic npn bipolar junction transistor (BJT).[20]

In addition, Ker et al. II discloses an n-well **44** is positioned to partially overlay and electrically couple with the n+ doped region **38**.[21] Beside the n+ doped region **38**, a p+ doped region **46** forms the electrical connection to p-well **32'**.[22] All the surfaces of the p+ regions **46** and **40** are capped by silicide material.[23] The areas of the n+ doped regions **36** and **38** are patterned by a photo mask **52** to block silicide material on their surfaces but the contact areas will be still covered with silicide.[24]

Further, Ker et al. II discloses the contacts **54** for the n+ doped regions **36** must be separated from poly-silicon gate **34** by a specific distance, as shown in FIG. 5A, to sustain a

[13] Ker et al. II at ABSTRACT.
[14] *Id.* at column 1, lines 16-17.
[15] *Id.* at column 1, lines 17-20.
[16] *Id.* at column 1, lines 20-23.
[17] *Id.* at column 1, lines 23-25.
[18] *Id.* at column 1, lines 26-28.
[19] *Id.* at column 1, lines 28-31.
[20] *Id.* at column 1, lines 31-34.
[21] *Id.* at column 1, lines 35-36.
[22] *Id.* at column 1, lines 36-37.
[23] *Id.* at column 1, lines 37-39.

higher ESD stress.[25] The shortest conductive path from the base of the npn BJT to the p+ doped region **46** must travel around n-well **44**, to take advantage of the higher resistance provided by spread resistor Rsub.[26]

However, it is respectfully submitted that Ker et al. II cannot overcome all of the deficiencies of the APA of **FIG. 2** regarding claim 7. In particular, Ker et al. II nowhere discloses, as claim 7 recites:

> providing a resistive path extending through an a single opening in a segmented conductive band from said well to substrate contacts located outside of said triple well and directly connected to a substrate, whereby the trigger voltage of the said ESD NMOSFET is reduced due to said resistive path between said substrate contacts and said I/O pad and
>
> wherein a first, second and third wells are formed in the substrate of the triple well CMOS structure,
>
> wherein the second well and third well of the triple well CMOS structure are completely isolated from a drain and source of the ESD NMOSFET by shallow trench isolation structures, and
>
> wherein the substrate contacts are located outside the first, second and third wells and directly connected to the substrate (emphasis added).

That is, neither Ker et al. II or APA of **FIG. 2** disclose: providing a resistive path **29b** extending through an a single opening **45**in a segmented conductive band **40a, 40b** from said well to substrate contacts located outside of said triple well and directly connected to a substrate, whereby the trigger voltage of the said ESD NMOSFET is reduced due to said resistive path between said substrate contacts and said I/O pad **11**, as similarly recited in amended claim 7 and 13 and as shown in the replacement sheet for amended **FIG. 4** above. In addition, neither Ker et al. II or APA of **FIG. 2** disclose: the second **37**well and third **38**well of the triple well CMOS structure are completely isolated from a drain **26** and source **25** of the ESD NMOSFET by shallow trench isolation structures **28, 33, 34, 42**, as similarly recited in amended claim 7 and as shown in the replacement sheet for amended **FIG. 4** above. Moreover, neither Ker et al. II or APA of **FIG. 2** disclose: the substrate contacts **44**, **50** are located outside the first **31**, second **37**

[24] *Id.* at column 1, lines 39-42.
[25] *Id.* at column 1, lines 43-45.
[26] *Id.* at column 1, lines 45-49.

and third **38** and directly connected to the substrate **41**, as similarly recited in amended claim 7 and as shown in the replacement sheet for amended **FIG. 4** above.

Further, it is respectfully submitted that Ker et al. II teaches away from the claimed invention. In particular, Ker et al. II discloses "an n-well is positioned to partially overlay and electrically couple with the n+ doped region **38**" and that "n+ doped regions 38 on the surface(s) of p-well(s) 32 provide the source (electrode)."[27]

Therefore, at least for the reasons above, it is respectfully submitted that neither the APA of **FIG. 2** or Ker et al. II, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention and that claim 7, and claims dependent thereon, patentably distinguish thereover.

Claim 9 was rejected under 35 U.S.C. 103(a) as unpatentable over APA of **FIG. 2** in view of Ker et al. II as applied to claim 7 above, and further in view of Ker et al. I. Applicants respectfully traverse the rejection.

Claim 9 is dependent on claim 7. Thus, at least for the reasons discussed above for claim 7, the APA of **FIG. 2** and Ker et al. II do not disclose all of the limitations of claim 9. In addition, the outstanding Office Action acknowledges deficiencies in the APA of FIG. 2 and Ker et al. II and attempts to cure those deficiencies with Ker et al. I. However, as discussed above, Ker et al. I cannot overcome all of the deficiencies of the APA of **FIG. 2** and Ker et al. II. In particular, Ker et al. I nowhere discloses, as claim 7 recites:

> providing a resistive path extending through an a single opening in a segmented conductive band from said well to substrate contacts located outside of said triple well and directly connected to a substrate, whereby the trigger voltage of the said ESD NMOSFET is reduced due to said resistive path between said substrate contacts and said I/O pad and
>
> wherein a first, second and third wells are formed in the substrate of the triple well CMOS structure,

[27] *See Ker et al. II* at column 4, lines 30-33 and 35-38.

wherein the second well and third well of the triple well CMOS structure are completely isolated from a drain and source of the ESD NMOSFET by shallow trench isolation structures, and

wherein the substrate contacts are located outside the first, second and third wells and directly connected to the substrate.

That is, at least for the same reasons discussed above for claim 1 and claim 7, Ker et al. I cannot overcome the deficiencies of the APA of **FIG. 2** and Ker et al. II.

Therefore, at least for the reasons above, it is respectfully submitted that none of the APAF, Ker et al. I, and Ker et al. II, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention, and that claim 9, and claims dependent thereon patentably distinguish thereover.

Conclusion

In view of the above amendment, applicant believes the pending application is in condition for allowance. If a fee is due, please charge the IBM Deposit Account No. 09-0456, under Order No. 21806-00158-US from which the undersigned is authorized to draw.

Dated: September 21, 2007

Respectfully submitted,

Electronic signature: /Myron Keith Wyche/
Myron Keith Wyche
Registration No.: 47,341
CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036
(202) 331-7111
(202) 293-6229 (Fax)
Attorney for Applicant